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High-T_c SNS Josephson Junctions: Moving Beyond Adolescence?

A.W. Kleinsasser and **K.A. Delin**
Center of Space Microelectronics Technology,
Jet Propulsion Laboratory,
California Institute of Technology,
Pasaden%CA91109, USA

***Abstract*—Attempts to develop high temperature superconductor (HTS) microelectronics have been limited by the immature nature of HTS circuit technology. Much of the present effort worldwide is based on superconductor-normal-superconductor (SNS) Josephson junctions (JJ's). Only within the past three years have SNS junctions been fabricated which can be interpreted with conventional proximity effect theory. We discuss the history and present status of** HTS SNS devices and the prospects **for producing a mature technology for practical applications.**

I. INTRODUCTION

SNS JJ's have received by far the most attention in the drive for practical HTS digital circuit technology. Challenging existing interpretations of the available data, we previously pointed out that virtually all early attempts to fabricate different types of HTS JJ's resulted in devices so similar in behavior that a common, usually unintended, mechanism was responsible for their properties [1], We subsequently provided the first evidence for proximity effect behavior in HTS junctions [2]. More recently, we published a thorough analysis of HTS SNS devices [3]. We turn here to a discussion of developments that will permit the application of SNS JJ's to future HTS microelectronic technology.

11. HISTORICAL PERSPECTIVE

The realization that Josephson effects occur naturally at grain boundaries in HTS materials led to engineered grain boundary junctions **(GBJ's)** on **bicrystal** substrates [4]. The physical mechanism of Josephson behavior in **GBJ's** has been the subject of much investigation [5]. Although **bi**crystals yield the most uniform and controllable HTS JJ's and provide the basis for SQUID products [6], they represent HTS **JJ** technology in its infancy. Because they are based on specially-prepared substrates, **bicrystal** devices are not readily extendible to full scale circuit applications.

The many attempts to fabricate a wide variety of thin-film HTS JJ's during the period 1988-1993 represent the "childhood" period of HTS **JJ** technology. **Bi-epitaxial** [7] and step-edge [8] GBJs extended the earlier **bicrystal** work, Other weak links and tunnel junctions were explored, but these investigations met with little practical success [3].

A significant breakthrough was the demonstration of HTS edge junctions. Edge junctions were the basis for a successful LTS circuit technology until supplanted by **trilayer** tunnel junctions, Interest in the edge structure was revived because HTS materials are highly **anisotropic.** Film growth occurs more naturally with the c-axis normal to the substrate. Not surprisingly, circuit-oriented HTS work uses c-axis-normal films, favoring in-plane junction geometries. As shown in Figure 1, an HTS edge junction is formed by first cutting a sloped edge in an **epitaxial** HTS film, which serves the base electrode. An **interlayer** and superconducting **counterelec**trode are deposited to complete the structure [9],[10]. Current flow is along the plane of the base electrode.

It was immediately recognized that HTS edge junctions would require **epitaxial interlayers.** Lattice matching is required in order to provide for **epitaxial** growth of the **counterelectrode** film. The use of ion milling as the basis for HTS edge junctions is problematic because sputtering of compound films typically results in **non-stoichiometric** surfaces in addition to lattice damage. The high temperature and oxygen atmosphere used in the **interlayer** and **counterelec**trode depositions apparently alleviate these problems. In addition, interdiffusion and physical property (e.g., thermal expansion coefficient) mismatches between the layers could degrade junction properties. Indeed, early results gave little indication of potential future applications. As late as 1993, the introduction of lattice-matched cubic oxide **interlayers**

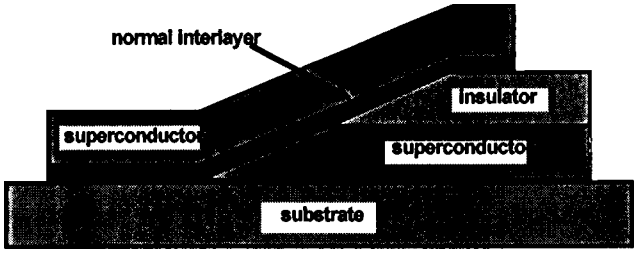

Fig. 1. Schematic of HTS edge junction structure. The sloped edge in the base-electrode-insulator bilayer is typically formed by ion milling. The epitaxial interlayer and counterelectrode are *grown* in a subsequent deposition. Current flow is predominantly in the plane of the base electrode.

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[11],[12] only resulted in junctions with large parameter spreads and GBJ-like behavior [3].

In a true SNS junction, the superconducting order parameter decays exponentially in N over a distance called the normal coherence length ξ_n, resulting in a critical current, I_c, which decreases exponentially with electrode separation, L, as $I_c \propto \exp[-L/\xi_n]$. Successful application of SNS theory to experiment dates back to the 1960's [13].

Most HTS edge junctions are only ***nominally SNS*** junctions (i.e., having normal metal interlayers and exhibiting Josephson behavior due to the proximity effect). Because BCS theory does not necessarily correctly describe HTS superconductors in detail, there are ample reasons, including large anisotropies, possible unconventional order parameter symmetry, and unusual boundary conditions, to question the applicability of conventional proximity effect theory to HTS junctions. These concerns may affect the details of theoretical predictions. However, there is little reason to doubt that superconducting correlations persist inside a normal metal at an SN interface, with the superconducting wavefunction in N decaying exponentially over the familiar coherence length given by an uncertainty principle-based argument, or that the basic idea of overlapping wavefunctions still underlies the Josephson effect.

Several mechanisms exist that could produce SNS critical currents below predicted values. Depairing effects (due, for example, to magnetic impurities) could reduce the correlation length to less than the normal coherence length, which remains an upper limit. The presence of extreme S-N mismatch or interracial potential barriers could greatly reduce, or even eliminate, any observable supercurrent,

Nevertheless, conventional proximity effect theory makes three clear and unambiguous predictions that may be taken as litmus tests of SNS behavior [3]: (1) I_c should exhibit a dramatic, exponential-like increase with decreasing T over a broad range below T_c. This temperature dependence should become steeper as electrode separation L increases, a clear qualitative indication of proximity effect behavior atypical of other junction types. (2) I_c should exhibit an exponential dependence on L, (3) The temperature-dependent decay length obtained from fitting I_c should be the calculated normal coherence length ξ_n, obtained unambiguously from interlayer parameters only, independent of SN boundary conditions, Establishing these features provides strong evidence for conventional proximity effect behavior, while failure to establish them provides strong evidence against an SNS interpretation.

Proximity effect theory was applied to early HTS junctions in a rather casual manner based on the assumed structure rather than the observed behavior, There was no real evidence for proximity effect behavior in most cases [3]. Nonmetallic transport in an interlayer renders conventional proximity effect theory inapplicable even in principle. Many nominally SNS HTS junctions fall into this category. Even in most HTS devices with metallic interlayers, the resistance is orders of magnitude larger than can be accounted for by the resistivity of the interlayer. This indicates a large SN interface resistance, The proximity effect can occur in SINIS structures as well as pure SNS ones, but drastic attenuation of the order parameter in typical barriers makes I_c negligible.

GBJ-like behavior is evident in most reported HTS junctions, and unintended pinholes in many nominally-SNS structures probably dominate transport [3]. From a practical point of view, many poorly-understood HTS junctions have been reported, with attendant poor process control.

111. PRESENT SITUATION

In order to develop HTS microelectronics, a full epitaxial multilayer circuit technology is required, with the junction component meeting several important criteria, Most obviously, the junctions must have acceptable electrical properties. Most applications require resistively shunted junction (RSJ) characteristics [14] with critical currents and resistances, R_n, in suitable ranges. Frequency response and output voltage are determined by the I_cR_n product. Parasitic inductance and capacitance must be acceptably small. Device-to-device spreads in these parameter values area major concern and stringency of requirements increases with circuit complexity. In the case of edge junctions, parameter values should be independent of edge orientation on-chip. Run-to-run variations and parameter stability are important for advancing from simple demonstrations to a manufacturable process.

Most present digital circuits are based on rapid single flux quantum (RSFQ) logic [15], with typical designs requiring products of gate critical current and inductance of roughly one flux quantum. This introduces the necessity of ground-planes. As recently as 1993, no viable candidate junction technology had been identified that appeared capable of meeting these and other practical criteria. Since that time, significant progress on the fabrication and physical analysis of HTS edge junction circuit technology has resulted in a maturing of the field into the present period of "adolescence."

In the case of edge devices, applying practical criteria to the junctions themselves yields important insights. The angle θ between the edge and the substrate in Fig. 1 must be shallow to allow epitaxial film growth without grain boundary formation (30° is typical, 90° being a vertical edge). Given a typical film thickness of 200 nm and assuming that the junction width exceeds 1 pm, the cross-sectional area of the junction is greater than 0.4 μm^2. Thermal fluctuations introduce the requirement that $\Phi_0 I_c >> kT$. For operation of temperatures on the order of 65 K, this and the requirement that $LI_c \approx \Phi_0$ mean that $I_c > 500\,\mu A$. Frequency response and output voltage considerations demand that $I_cR_n > 300\,\mu V$ in most circuits. This implies that $R_n > 0.6\,\Omega$ or $R_nA > 2.4 \times 10^{-9}\,\Omega\text{-cm}^2$. Since interlayers in good devices are less than 20 nm thick, the required interlayer resistivity is $\rho_n > 1\,m\Omega\text{-cm}$.

In the development of HTS JJ's from "childhood" to "adolescence," the designation "SNS" has been often referred to any device not behaving as a conventional tunnel junction. However, proximity effect theory applies only to metals and the requirement that $\rho_n > 1$ mΩ-cm implies a non-metallic material. From a practical point of view, the edge geometry is a poor one for pure SNS (as distinct from SINIS) devices, One approach to fabricating practical HTS edge junctions is to abandon metallic interlayers entirely. We will designate as S1'S junctions which are not governed by direct tunneling (i.e., S1S) but nevertheless have non-metallic interlayers.

Non-metallic-interlayer HTS edge junctions are not new [9], but device analysis has typically used the SNS framework, Significant recent theoretical interest in the behavior of S1'S junctions [16] and re-examination of the implications of proximity effect theory [1],[3],[17] have caused a departure from this approach. On the experimental side, progress in non-SNS HTS edge junctions has been steady. A thorough review of the literature is beyond the scope of this paper and brief references must suffice. Most S1'S edge junctions employ interlayers of $PrBa_2Cu_3O_{7-x}$ [9]. The contributions of the Twente University group in this area have been substantial[18], as have those from others [3],[19]-[22]. In addition to improvements in junction properties and fabrication processes, there has been significant progress in understanding their electrical behavior [19], [23].

There are approaches to producing practical HTS edge junctions that circumvent the non-metallic interlayer requirement. The most obvious is to scale device widths down to submicrometer dimensions. Unfortunately, this is likely to make parameter spreads significantly worse. An alternative is to employ use SINIS, rather than pure SNS, junctions. An insulator at an SN interface drastically reduces the proximity effect, resulting in negligible critical currents and I_cR_n products. This can be avoided by using inhomogeneous interfaces or SINS junctions [3],[24].

Neither the strong resistivity-based argument against even considering pure SNS edge junctions nor failure to fabricate them has prevented research on such devices from proceeding. Early failures with the epitaxial edge junction approach led to attempts to better match interlayer and electrodes, not just in lattice parameters but in chemical composition [25] and thermal expansion coefficient [26]. Attempts to achieve true SNS devices by this approach were successful when $YBa_2Cu_3O_{7-x}$ edge junctions were fabricated with $Y_{0.7}Ca_{0.3}Ba_2Cu_3O_{7-x}$ [27], [28]. Analysis in terms of conventional proximity effect theory found excellent quantitative agreement between calculated and experimental $I_c(T;L)$ [2]. This agreement was the first convincing evidence of proximity effect behavior in HTS SNS junctions, providing strong support for applying conventional proximity effect theory to them,

In the case of experiments with $YBa_2Cu_{2.79}Co_{0.21}O_{7-x}$ interlayers, also aimed at eliminating interracial resistance in HTS SNS structures [27], [29], we calculated currents of the right order of magnitude exhibiting the expected qualitative features [2]. In this case, only the first two of the aforementioned litmus tests were successful, the measured decay length being significantly longer than the calculated ξ_n.

As expected, the resistances of these doped-interlayer devices were too small to be considered practical. It is therefore ironic that extensions of this work led to practical HTS edge junctions, Today, edge junctions with Co-doped $YBa_2Cu_3O_{7-x}$ interlayers are the most heavily-investigated HTS devices for microelectronic applications. This occurred because attempts to duplicate the initial $YBa_2Cu_{2.79}Co_{0.21}O_{7-x}$ devices resulted in very similar junctions, passing two of the three litmus tests for SNS behavior. However, device resistances were higher by up to an order of magnitude [30]. These promising results have been tentatively interpreted by invoking an SINIS (or perhaps SINS) structure with inhomogeneous interfaces, effectively reducing the active device area and increasing R_n without affecting I_cR_n [24]. It is emphasized that this explanation and the proximity effect model for the pure SNS-like Co-doped devices require a coherence length in N that is anomalously long (violating the third litmus test for proximity effect behavior), suggesting an interesting topic for further investigation.

Despite an incomplete understanding of the basic transport physics in these devices, strong interest in practical circuit applications has driven several developments including significant reductions in parameter spreads, orientation-independent edge formation procedures, and the demonstration of these junctions on superconducting groundplanes [31],[32]. Shortcomings in the present process include parameter spreads still too wide for useful circuits, poor run-to-run reproducibility, and the disparity in results between various groups, some reporting SNS-like devices [32], [33], others SINIS-like ones [31],[34]. Although the technology is far from mature, recent results represent clear engineering steps in the right direction and significant advances over earlier physics-oriented junction work.

IV. FUTURE DIRECTIONS

There is reason to believe that HTS SNS junctions are ready to mature beyond the period of "adolescence" into "adulthood." This stage will be reached when stable junctions having acceptable parameters with narrow spreads ($\sigma <$ 5-10?4o) on superconducting groundplanes are routinely available and incorporated into functional gates suitable for digital circuits. Leading contenders for junction technology are SINIS edge junctions with Co-doped $YBa_2Cu_3O_x$ interlayers and S1'S junctions with $PrBa_2Cu_3O_x$-based interlayers. There is clearly room, however, for significant innovations in interlayer materials, edge processing, and other aspects of device and circuit fabrication,

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